REMARKS

Claims 12 and 17 are amended. Claims 47-88 are added. Claims 1-88 are in the application for consideration.

The title and independent claims 12 and 17 have been amended to delete reference to volatility.

Claims 47-88 are added. Each of the independent claims included in claims 47-88 is patterned after the already allowed independent claims, but deletes reference to voltage or current controlled resistance setable semiconductive material, and instead refers to a chalcogenide material. The specification as filed clearly supports a chalcogenide comprising material.

This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: 8-22-02

By: _____
Mark S. Matkin
Reg. No. 32,268

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/921,518
Filing Date ..... August 1, 2001
Inventor ..... John T. Moore
Assignee ..... Micron Technology, Inc.
Group Art Unit 2818
Examiner ..... Phuc T. Dang
Attorney's Docket No. MI22-1669
Title: Method Of Forming Integrated Circuitry, Method Of Forming Memory Circuitry, And Method Of Forming Random Access Memory Circuitry

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING SUPPLEMENTAL PRELIMINARY AMENDMENT FOLLOWING AUGUST 1, 2002 RCE FILING

In the Title:

The title has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Method Of Forming Integrated Circuitry, Method Of Forming Memory Circuitry, And Method Of Forming ~~Non-Volatile~~ Random Access Memory Circuitry

In th Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

12. (Amended) A method of forming ~~non-volatile~~ random access memory circuitry comprising:

forming a plurality of memory cell access transistor gates over a semiconductor substrate;

forming a plurality of metal interconnect lines over the substrate and the memory cell access transistor gates;

after forming the conductive metal interconnect lines, forming respective first memory cell electrodes in electrical connection with respective memory cell access transistors incorporating the memory cell access transistor gates;

forming voltage or current controlled resistance setable semiconductive material in electrical connection with the respective first electrodes; and

forming at least one second memory cell electrode in electrical connection with the voltage or current controlled resistance setable material.

17. (Amended) A method of forming at least two ~~non-volatile~~ random access memory cells comprising:

forming at least two memory cell wordlines over a semiconductor substrate, the two memory cell wordlines being proximate one another;

forming at least one metal bit line in electrical connection with active area of the semiconductive substrate which is between the two memory cell wordlines;

after forming the metal bit line, forming respective first memory cell electrodes in electrical connection with active area of the semiconductive substrate on respective lateral outer sides of the two wordlines;

forming voltage or current controlled resistance setable semiconductive material in electrical connection with the respective first electrodes; and

forming a second memory cell electrode in electrical connection with the voltage or current controlled resistance setable material, the second memory cell electrode being common to the two memory cells being formed.

New claims 47-88 are added.

-END OF DOCUMENT-